Preliminary Reliability Report

General Information	
Product Line	*UAV5*
Product Description	*batSPIN*
Product division	*I&PC*
Package	*VFQFPN 16 3x3x1.0*
Silicon process technology	*BCD8sP*

Locations	
Wafer fab location	*AGRATE*
Assembly plant location	*UTAC Thai Limited*
Preliminary Reliability assessment	*Positive*

DOCUMENT HISTORY

Version	Date	Pages	Author	Comment
1.0	18-Oct-18	14	M. Benzoni	Original document

Approved by

A. Paratore

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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q100	: Stress test qualification for integrated circuits
0061692	: Reliability tests and criteria for qualifications

2 RELIABILITY EVALUATION OVERVIEW

2.1 Objectives

This report contains the reliability evaluation of UAV5 device diffused in ST AGRATE and assembled in VFQFPN 16 3x3x1.0 in UTAC Thai Limited.
According to Reliability Qualification Plan, considering that UAV5 assembled in ST CALAMBA is already qualified and in production, below the list of the trials performed:

Die Oriented Tests (performed on UAV5 assembled in Calamba)

- High Temperature Operating Life

Package Oriented Tests

- Preconditioning
- Temperature Cycling
- Autoclave
- High Temperature Storage Life
- Temperature Humidity Bias *(performed on UAV5 assembled in Calamba)*

Electrical Characterization

- ESD resistance test
- LATCH-UP resistance test *(performed on UAV5 assembled in Calamba)*

2.2 Conclusion

The preliminary reliability results of the trials performed on UAV5 diffused in ST AGRATE and assembled in VFQFPN 16 3x3x1.0 in UTAC Thai, have shown that the devices behave correctly against environmental tests.

Temperature Cycling and High Temperature Storage Life trials on three assembly lots have to be completed.

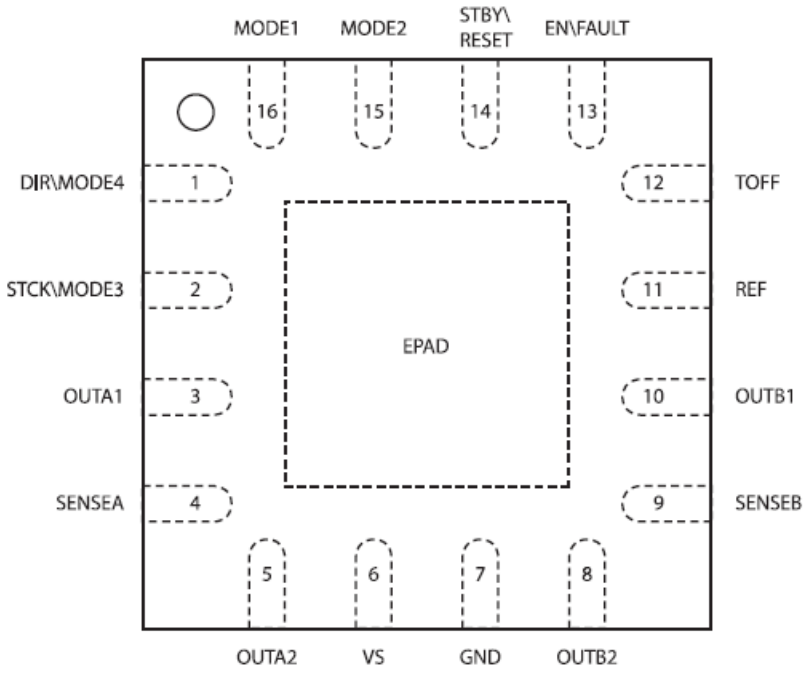
3 DEVICE CHARACTERISTICS

3.1 Device description

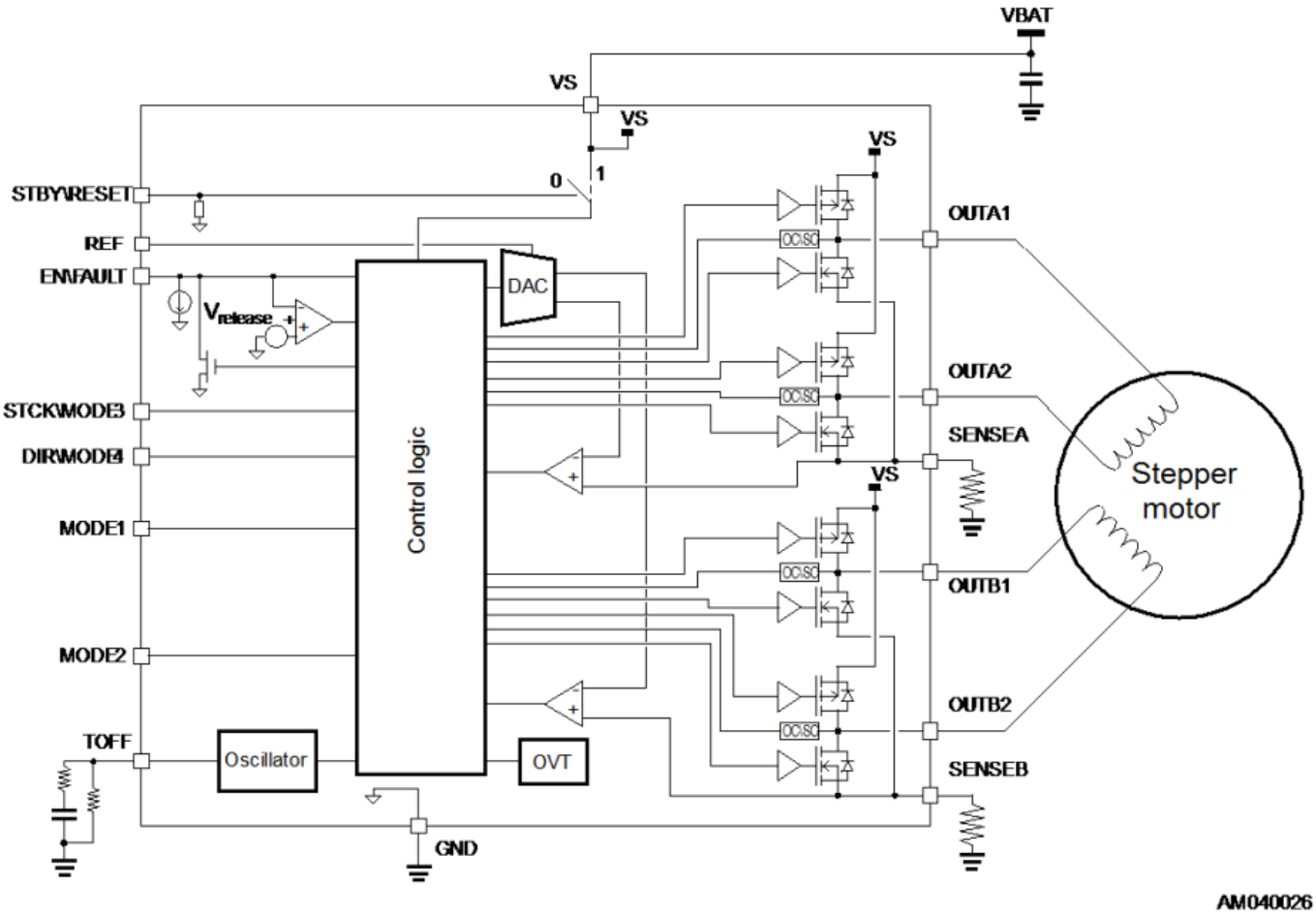
3.1.1 Generalities

The UAV5 is a stepper motor driver which integrates, in a small QFN 3 x 3 mm package, both control logic and a low RDS(on) power stage. The integrated controller implements PWM current control with fixed OFF time and a microstepping resolution up to 1/256th of a step. The device is designed to operate in battery powered scenarios and can be forced into a zero consumption state, allowing a significant increase in battery life.

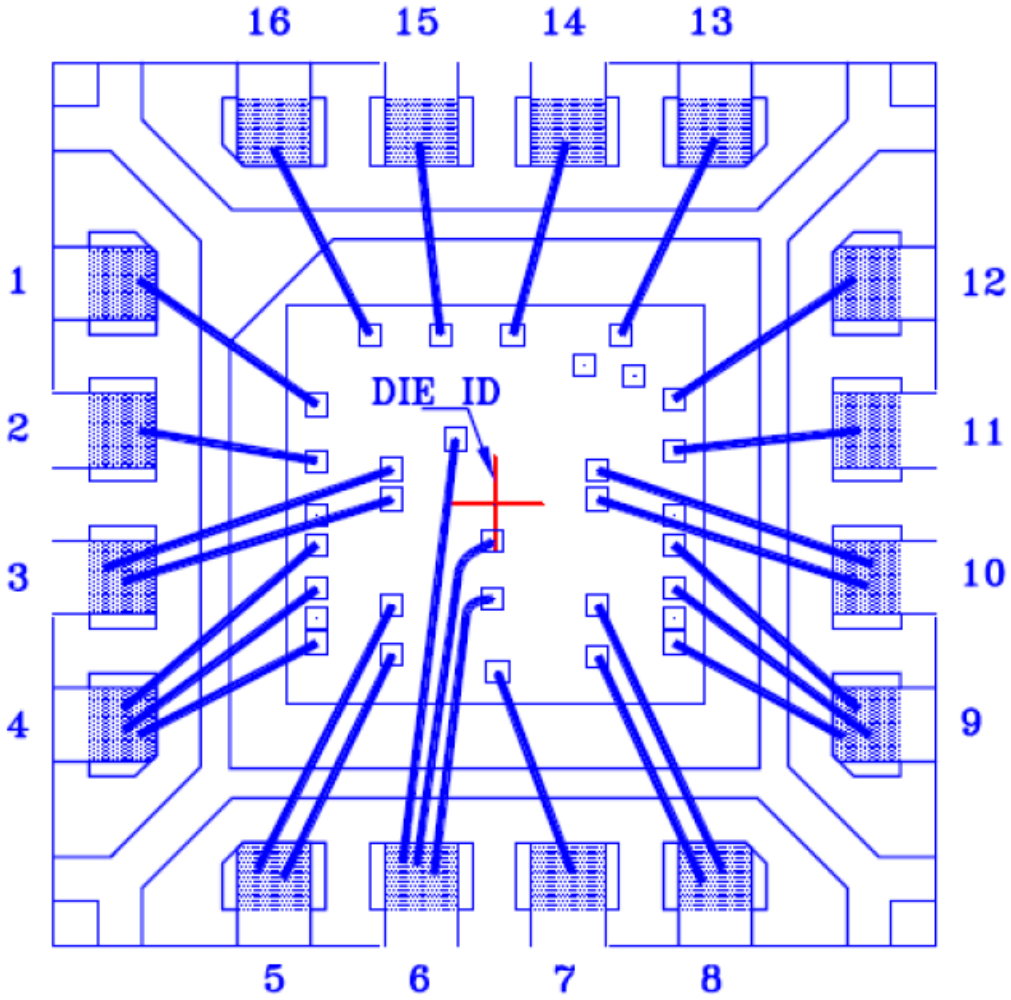
3.1.2 Pin connection (Top view)



3.1.3 Block diagram



3.1.4 Bonding diagram



3.2 Traceability

Wafer fab information	
Wafer fab manufacturing location	*AGRATE*
Wafer diameter	*8 inch*
Wafer thickness	*280um*
Silicon process technology	*BCD8sP*
Die finishing back side	*Cr / NiV / Au*
Die size	*1357 x 1422um*
Bond pad metallization layers	*NiPd*
Passivation	*NITRIDE*
Metal levels	*4*

Assembly Information	
Assembly plant location	*UTAC Thai Limited*
Package description	*VFQFPN 16 3x3x1.0*
Molding compound	*G700LTD*
Wires bonding materials/diameters	*Cu / 1.2mil*
Die attach material	*8200T*
Lead solder material	*NiPdAu*

4 TESTS RESULTS SUMMARY

4.1 LOTs information

Lot ID #	Silicon Rev.	Assy Plant	Diff. Plant
1	UAV5AA	ST Calamba	ST Agrate
2	UAV5AB	ST Calamba	ST Agrate
3	UAV5AB	ST Calamba	ST Agrate
4	UAV5AE	ST Calamba	ST Agrate
5	UAV5AC	UTAC Thailand	ST Agrate
6	UAV5AC	UTAC Thailand	ST Agrate
7	UAV5AC	UTAC Thailand	ST Agrate

4.2 Results summary (Assy Calamba)

Die Oriented Tests *(performed on UAV5 assembled in Calamba)*							
Test	**Method**	**Conditions**	**Failure/SS**			**Duration**	**Note**
			Lot 1	**Lot 2**	**Lot 3**		
HTOL	High Temperature Operating Life (Static)						
		Tjmax=150°C Vs=11V	**-**	**0/77**	**0/77**	**1000h**	**-**
HTOL	High Temperature Operating Life (Dynamic)						
		Tjmax=150°C Vs=10V	**-**	**0/77**	-	**1000h**	**-**

Package Oriented Tests *(performed on UAV5 assembled in Calamba)*							
Test	**Method**	**Conditions**	**Failure/SS**			**Duration**	**Note**
			Lot 1	**Lot 2**	**Lot 3**		
PC	Pre-Conditioning: Moisture sensitivity level 3						
		40h 60°C/60% - 3 reflow PBT 260°C	**0/154**	**0/77**	-		**-**
THB	Temperature Humidity Bias						
	PC before	**Ta=85°C/85%RH**	**-**	**0/77**	-	**1000h**	**-**
AC	Autoclave						
	PC before	**121°C 2atm**	**0/77**	**-**	**-**	**96h**	**-**
TC	Temperature Cycling						
	PC before	**Temp. range: -65/+150°C**	**0/77**	**-**	**-**	**2000cy**	-
HTSL	High Temperature Storage						
	No bias	**Tamb=150°C**	**0/45**	**-**	**-**	**1000h**	**-**

	Electrical Characterization Tests*(performed on UAV5 assembled in Calamba)*					
Test	**Method**	**Conditions**	**Failure/SS**		**Duration**	**Note**
			Lot 4			
ESD	Electro Static Discharge					
	Human Body Model	**+/- 2kV**	**0/3**	**-**	**-**	**-**
	Charge Device Model	**+/- 500V**	**0/3**		**-**	**-**
LU	Latch-Up					
	Over-voltage and Current Injection	**Tamb=125°C Jedec78**	**0/6**	**-**	**-**	**-**

4.3 Test Plan and preliminary results summary (Assy UTAC Thailand)

Package Oriented Tests							
Test	**Method**	**Conditions**	**Failure/SS**			**Duration**	**Note**
			Lot 5	**Lot 6**	**Lot 7**		
PC	Pre-Conditioning: Moisture sensitivity level 3						
		192h 30°C/60% R.H - 3 reflow PBT 260°C	**0/150**		-		**-**
AC	Autoclave						
	PC before	**121°C 2atm**	**0/25**	**0/25**	**0/25**	**96h**	**-**
TC	Temperature Cycling						
	PC before	**Temp. range: -65/+150°C**	**(*) 0/25**	**(*) 0/25**	**(*) 0/25**	**2000cy**	**(*) Results @ 200cy readout**
HTSL	High Temperature Storage						
	No bias	**Tamb=150°C**	**(*) 0/25**	**(*) 0/25**	**(*) 0/25**	**1000h**	**(*) Results @ 500h readout**

(*) Preliminary data

	Electrical Characterization Tests					
Test	**Method**	**Conditions**	**Failure/SS**		**Duration**	**Note**
			Lot 7	**-**		
ESD		Electro Static Discharge				
	Charge Device Model	**+/- 500V**	**0/3**	-	**-**	**-**

5 TESTS DESCRIPTION & DETAILED RESULTS

5.1 Die oriented tests

5.1.1 High Temperature Operating Life

This test is performed like application conditions in order to check electromigration phenomena, gate oxide weakness and other design/manufacturing defects put in evidence by internal power dissipation.

The flow chart is the following:

- Initial testing @ Ta=25°C
- Check at 168 and 500hrs @ Ta=25°C
- Final Testing (1000 hr.) @ Ta=25°C

5.2 Package oriented tests

5.2.1 Pre-Conditioning

The device is submitted to a typical temperature profile used for surface mounting, after a controlled moisture absorption.
The scope is to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.

5.2.2 High Temperature Storage

The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.
The scope is to investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding

5.2.3 Thermal Cycles

The purpose of this test is to evaluate the thermo mechanical behavior under moderate thermal gradient stress.
Test flow chart is the following:
TEST CONDITIONS:

- Initial testing @ Ta=25°C.
- Readout @ 200,500, 1000 cycles.
- Final Testing @ 2000 cycles @ Ta=25°C.

TEST CONDITIONS

- Ta= -65°C to +150°C(air)

5.2.4 Autoclave

The purpose of this test is to point out critical water entry path with consequent corrosion phenomena related to chemical contamination and package hermeticity.
Test flow chart is the following:

- Initial testing @ Ta=25°C.
- Final Testing (96hrs) @ Ta=25°C.

TEST CONDITIONS:

- P=2.08 atm
- Ta=121°C
- test time= 96 hrs

5.2.5 Temperature Humidity Bias

The test is addressed to put in evidence problems of the die-package compatibility related to phenomena activated in wet conditions such as electro-chemical corrosion.
The device is stressed in static configuration approaching some field status like power down. Temperature, Humidity and Bias are applied to the device in the following environmental conditions => Ta=85°C / RH=85%.
Input pins to Low / High Voltage (alternate) to maximize voltage contrast.
Test Duration 1000 h.

The flow chart is the following:

- Initial testing @ Ta=25°C
- Check @ 168 and 500hrs
- Final Testing (1000 hr.) @ Ta=25°C

5.3 Electrical Characterization Tests

5.3.1 Latch-up

This test is intended to verify the presence of bulk parasitic effects inducing latch-up.
The device is submitted to a direct current forced/sinked into the input/output pins. Removing the direct current no change in the supply current must be observed.

Stress applied:

condition	NEG. INJECTION	POS. INJECTION	OVERVOLTAGE
IN low: 0V	-100mA	Inom+100mA Note1	1.5 x VDD or MSV or AMR, whichever is less
IN high: 3.6V	-100mA	Inom+100mA Note2	1.5 x VDD or MSV or AMR, whichever is less

5.3.2 E.S.D.

This test is performed to verify adequate pin protection to electrostatic discharges.
The flow chart is the following:

- Initial testing @ Ta=25°C
- ESD discharging @ Ta=25°C
- Final Testing @ Ta=25°C

TEST CONDITIONS:

- **Human Body Model** — ANSI/ESDA/JEDEC STANDARD JES001
  CDF-AEC-Q100-002
- **Machine Model** — JEDEC STANDARD EIA/JESD-A115
  CDF-AEC-Q100-003
- **Charge Device Model** — ANSI/ESD STM 5.3.1 ESDA – JEDEC JESD22-C101
  CDF-AEC-Q100-011